MONOLITHIC GATED DELAY LINE OSCILLATOR (SERIES 3D7702)

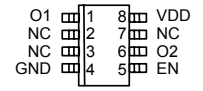
RoHS Compliant

data delay devices, inc.

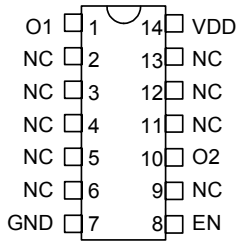
FEATURES

- All-silicon, low-power CMOS technology
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- **Frequency range:** 0.3MHz through 100MHz
- **Frequency tolerance:** 0.5% typical
- **Temperature stability:** ±1.5% typical (-40C to 85C)
- **Vdd stability:** ±0.5% typical (4.75V to 5.25V)
- 14-pin DIP available as drop-in replacements for hybrid delay line oscillator (DLO32F)

PACKAGES



3D7702Z-xx SOIC-8



3D7702-xx DIP-14
3D7702K-xx NC pins removed

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7702 Delay Line Oscillator product family consists of fixed-frequency CMOS integrated circuit oscillators. Each package contains a single oscillator, which is gated and can therefore be synchronized to an external signal. The device frequency can range from 0.3MHz through 100MHz. The 3D7702 has two outputs that are 180° out-of-phase when the oscillator is running, and can be used as a drop-in replacement for the DLO32F hybrid oscillator. The 3D7702 is TTL- and CMOS-compatible, capable of driving ten 74LS-type loads. It is offered in a standard 14-pin auto-insertable DIP and a space saving surface mount 8-pin SOIC package.

PIN DESCRIPTIONS

EN	Oscillator Enable
O1	Oscillator Output 1
O2	Oscillator Output 2
VDD	+5 Volts
GND	Ground

TABLE 1: PART NUMBER SPECIFICATIONS

DASH NUMBER	OUTPUT FREQUENCY (MHz)	
	25C Vdd=5.00V	-40C to 85C 4.75<Vdd<5.25
-0.3	0.3 ± 0.002	0.3 ± 0.008
-0.4	0.4 ± 0.002	0.4 ± 0.010
-0.5	0.5 ± 0.003	0.5 ± 0.013
-0.75	0.75 ± 0.004	0.75 ± 0.019
-1	1.0 ± 0.005	1.0 ± 0.025
-2	2.0 ± 0.010	2.0 ± 0.050
-2.5	2.5 ± 0.013	2.5 ± 0.063
-3	3.0 ± 0.015	3.0 ± 0.075
-4	4.0 ± 0.020	4.0 ± 0.100
-5	5.0 ± 0.025	5.0 ± 0.125
-7.5	7.5 ± 0.038	7.5 ± 0.188
-10	10.0 ± 0.05	10.0 ± 0.25
-20	20.0 ± 0.10	20.0 ± 0.50
-25	25.0 ± 0.13	25.0 ± 0.63
-30	30.0 ± 0.15	30.0 ± 0.75
-40	40.0 ± 0.20	40.0 ± 1.00
-50	50.0 ± 0.25	50.0 ± 1.25
-75	75.0 ± 0.38	75.0 ± 3.75
-100	100.0 ± 0.50	100.0 ± 7.00

NOTE: Any dash number between 0.3 and 100 not shown is also available as standard.

APPLICATION NOTES

OPERATIONAL DESCRIPTION

The 3D7702 delay line oscillator architecture is shown in Figure 1. The internal delay line is composed of a number of delay cells connected in series and is compensated for thermal and supply voltage variations. A low-going edge on the EN input starts the oscillator, with the O2 output responding immediately. The O1 output is delayed by ½ cycle. The response of the output when the oscillator is disabled depends on the status of O2 when the EN signal goes high, as shown in Figure 2. If O2 is low, it will remain low, and the final pulse on O1 will be ½ of the period. If O2 is high, it will go low as soon as EN goes high, and the final pulse on both outputs will have a width smaller than ½ the period.

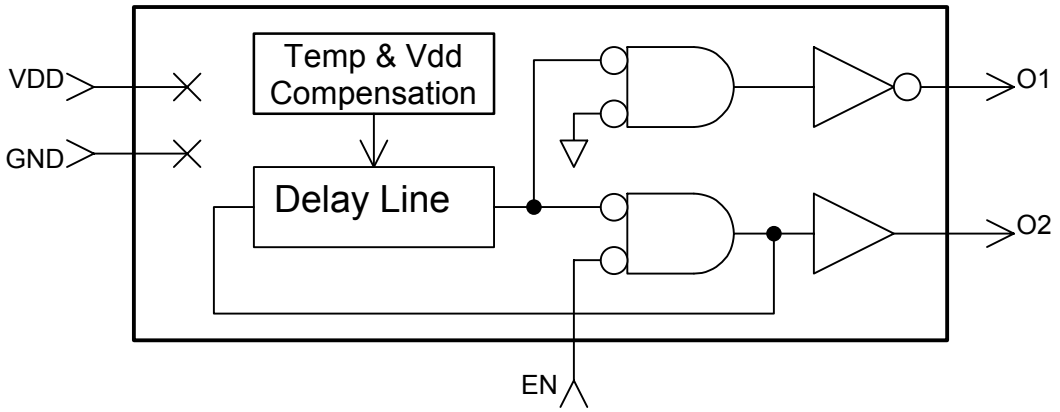


Figure 1: 3D7702 Functional Diagram

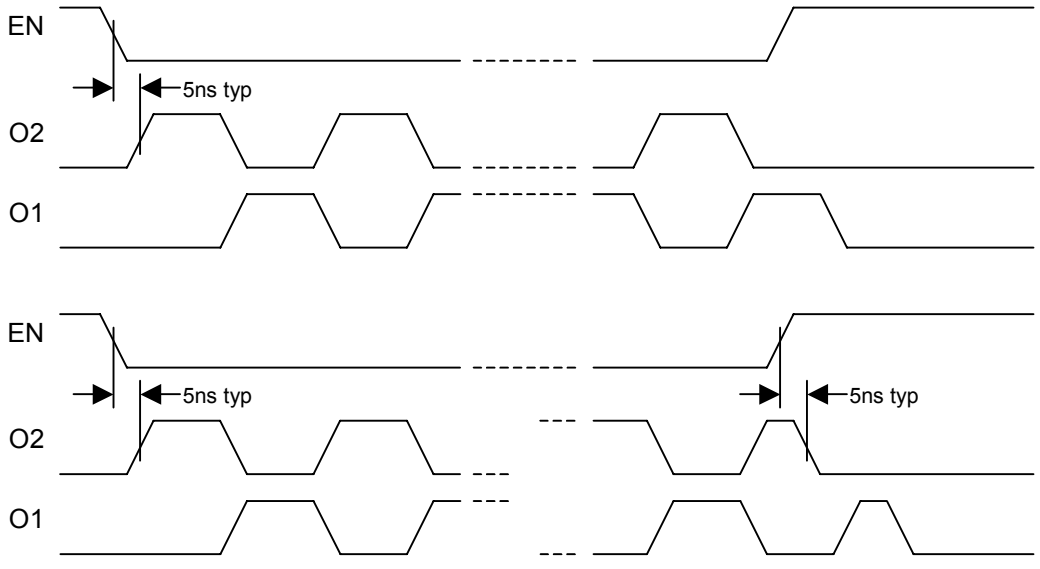


Figure 2: 3D7702 Timing Diagrams

APPLICATION NOTES (CONT'D)

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The monolithic 3D7702 oscillator utilizes novel and innovative compensation circuitry to minimize the frequency variations induced by fluctuations in power supply and/or temperature.

The thermal coefficient is reduced to 250 PPM/C, which is equivalent to a variation, over the -40C to 85C operating range, of ±1.5% from the room-temperature frequency setting. The power supply coefficient is reduced, over the 4.75V to 5.25V operating range, to ±0.5% of the frequency setting at the nominal 5.0VDC power supply. These specifications hold for the lower frequencies only. For higher dash numbers, the variations will be slightly greater, as noted in Table 1. **It is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.**

DEVICE SPECIFICATIONS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-1.0	1.0	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		3.5	5.5	mA	
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}			1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}			1.0	µA	$V_{IL} = 0V$
High Level Output Current	I_{OH}		-35.0	-4.0	mA	$V_{DD} = 4.75V$ $V_{OH} = 2.4V$
Low Level Output Current	I_{OL}	4.0	15.0		mA	$V_{DD} = 4.75V$ $V_{OL} = 0.4V$
Output Rise & Fall Time	T_R & T_F		2.0	2.5	ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 2 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/output (pf)
F = Device frequency (GHz)

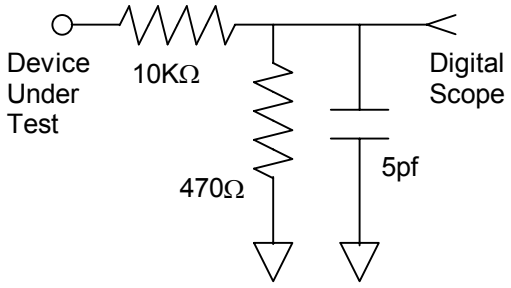
Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 5.0V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V
)

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

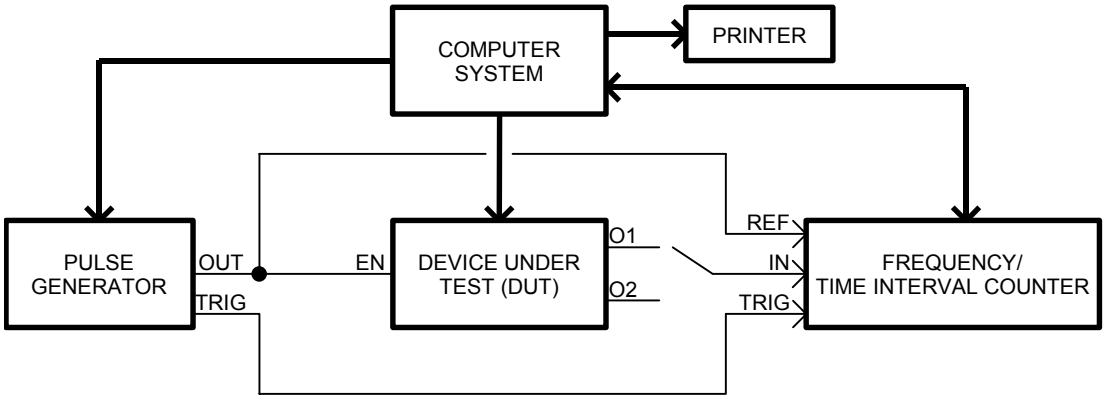


Figure 3: Test Setup

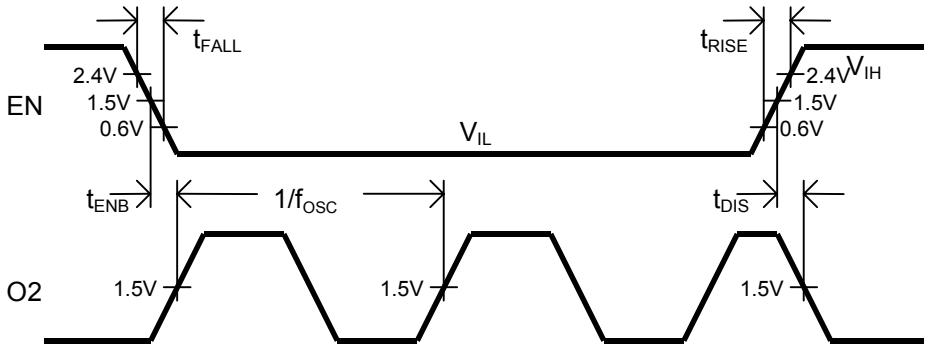


Figure 4: Timing Diagram